

System Requirements of a Stationary-Head Multi-Track Recorder

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Abstract—We report on the design considerations of stationary-head multi-track magnetic recorders. We will focus on the particular reasons for adopting the rate 8/10, dc-free recording code, the full-response detection method, and the clock recovery circuitry. Implementation issues of the channel chip, particularly related to cost and power consumption, will be addressed. A new multi-track Phase-Lock Loop (PLL) was developed, in order to improve the recorder's robustness against time-base variations.

I. INTRODUCTION

There are many different kind of magnetic recorders, and it is therefore difficult to provide a unified approach to the signal processing and coding techniques used in those devices. There is a considerably sharp distinction between the signal processing/code design used in rigid-disk devices and tape recorders. Tape recorders, in turn, can be distinguished into two main categories: rotary-head and stationary-head systems. Examples of state-of-the-art digital rotary-head recorders for consumer use are the DAT [1] and Scoopman. Examples of stationary-head recorders include the Digital Compact Cassette (DCC) [2] audio recorder and the Quarter Inch Cassette (QIC) drive used as data streamer. The system characteristics of rotary relative to stationary-head tape recorders have lead to significantly different approaches to the signal processing and code design. Our objective in this paper is to present the requirements of advanced signal processing related to stationary-head recorders. We commence with a brief description of the system. Next we turn our attention to the data detection techniques and related implementation issues adopted in a state-of-art recorder. Power consumption and cost are key issues as the state-of-the-art recorder described is intended for a high-volume market.

II. DESCRIPTION OF THE SYSTEM

The system studied during our experiments is an 8-track digital recorder, whose main parameters are listed

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TABLE I
Main parameters of the multi-track recorder

tape speed	4.76 cm/sec
tape width	3.78 mm
channel bit rate/track	96 kbit/sec
track width (write)	185 μm
track width (read)	70 μm .

below.

Given the tape speed and channel bit rate, we easily find that the channel bit length is $0.5\mu\text{m}$. The wave length is approximately $1\mu\text{m}$. The recorder is not equipped with an erase head, and recording of new information is accomplished by direct over writing the old information. A severe disadvantage of this technique is that the old information is not fully erased causing over-write noise. Details of the error correction and source coding system are omitted as their description is outside the scope of this paper. Play-back is done with an 8-track magneto-resistive (MR) yoke-type head.

A. Tape format

The binary-valued sequences written on tape are divided into blocks of information called *tape frames*. Each tape frame consists of 32 tape blocks plus a pattern called *inter frame gap*. The nominal length of the inter frame gap is 64. The length may vary to some extent in order to accommodate source data speed variations during recording. Each tape block, in turn, consists of 51 10-bit tuples called symbols. The 10-bit tuples are generated under the rules of the rate 8/10 code (ETM) scheme (see later for its details). Three of the 51 10-bit tuples are used for block synchronization and frame identification. The remaining, 48, 10-bit tuples carry the parity check and user information.

B. ETM channel code

The Eight-to-Ten code (ETM) is a member of the family of dc-balanced codes [3]. Under ETM rules, the source sequence is translated into a sequence whose low-frequency components are rejected. The main rationales for adopting a dc-free code are: over-write noise and simplicity (both cost and power consumption) of the read

equalization circuitry. Over-write noise is dominant in the low-frequency region. Rejection of these low-frequency disturbances is easily accomplished by high-pass filtering. As the signal itself has no low-frequency components, the signal is not distorted by this filtering. The second reason for adopting a dc-free code is related to the read head response. The MR-head used is a yoke-type head which shows response at the low-frequency end. However, the impulse response is asymmetrical, see Figure 1, so that the head's phase response at the low-frequency end is far from linear. Electronic phase compensation would entail a prohibitively large (digital) filter. An obvious drawback of the ETM code is the extra overhead of 25 percent.

The source signal is assumed to be partitioned into words of eight bits that are translated by the channel encoder into the channel symbols. Thereafter, the channel symbols are recorded sequentially on the recording medium. The ETM codebook comprises two pages, $A(\sigma_0)$ and $A(\sigma_1)$, where σ_0 and σ_1 denote the two encoder states. Each page has 256 entries which enables a one-to-one state-dependent encoding. Depending on the specific transmitted codeword, the encoder state alters from state or remains in the same state. The code was constructed to allow a simple low-cost encoding and decoding. The channel sequence takes on at most six digital sum values, the maximum run-length is five channel symbols, and state-independent block decoding is possible. On decoding, no use is made of the actual value of the digital sum or information of adjacent codewords. As a result, error propagation is limited to a single decoded byte. It can be calculated that the number of allowed codewords emanating from σ_0 and terminating in σ_0 and σ_1 is 197 and 155, respectively. From state σ_1 there are 155 and 131 codewords terminating in σ_0 and σ_1 , respectively. We conclude that the minimum number of codewords leaving a state $131+155 = 286$. A few candidate words were discarded to make it possible to use a unique 10-bit sync pattern.

III. DETECTION METHOD

The signal retrieved from the tape is heavily distorted by the dispersive read-out process. Also various noise and interference sources have added their undesirable components to the read signal. The electronic process that transforms the distorted signal into a clocked binary signal is called (*bit*) *detection*. There are a large variety of detection methods. The detection method involves among others the shape of the overall frequency characteristic. In *full-response* detection, also called write current restoration, a signal is produced resembling the waveform written on the tape. The zero crossings of the restored waveform occur at regular intervals which provide information for the time base correction. The full-response detection scheme is characterized by the fact that intersymbol interference (ISI) at the sampling instants is small or even

absent. In equalization schemes based on partial-response (PR) systems, ISI is not necessarily treated as an undesirable phenomenon but they permit *controlled* intersymbol interference whose known effects are compensated at the data detector. The advantage of such PR systems, relative to full-response systems, is a reduced bandwidth requirement resulting in improved additive noise margin. Specifically, Class IV PR systems have been used in rigid-disk drives and rotary-head tape recorders for improving the information density [4]. There are, however, a few impediments in PR detection, which limit its usefulness in stationary-head tape recorders. The first weakness is that certain, worst-case, patterns may cause difficulties. Long sequences of like symbols, for example, can easily foil the timing recovery or the adaptive amplitude control whose design usually rests on the assumption that the signals are stationary. Accurate clocking of PR systems is paramount as they are more sensitive to timing errors than full-response channels of the same excess bandwidth. Amplitude control is a prerequisite in PR systems as the multi-level signals present in PR systems can only be detected by prior knowledge of the signal's amplitude. In rigid disk drives, dedicated parts of the tracks are used for "training sequences" that provide information enabling a rapid adaptation to changing channel parameters. In rotary-head systems, preamble sequences situated at the start of each track, serve in a similar function. The usage of such dedicated sectors in stationary-head tape recorders is not a viable option. The third weak spot of PR detection is its sensitivity to time-base variations. In the stationary-head drive at hand, the low tape velocity, 4.76 cm/s, is the source of relatively large tape velocity variations. In particular during periods of severe shocks or vibration, for example during portable use, speed variations can easily exceed 20 percent of the nominal value. The eye width of PR systems has been computed by Kabal and Pasupathy [5] and is about 36% of the eye width of a full response channel. Experiments showed, for the detection system used, that a tape speed decrease or increase of 10 % can be tolerated for a full-response system. The PR system is much more sensitive to speed tolerance as it breaks down at a speed deviation of only 5 %. A careful analysis and weighing of the various merits and demerits mentioned above have lead to the adoption of full-response detection.

The small signal emerging from the read head is amplified, and after appropriate filtering, it is forwarded to the A-to-D converter. The analog filter serves two purposes, namely anti-aliasing and pre-equalization. The pre-equalization (the term pre-equalization should not be confused with write equalization.) is essentially a filter that boosts the high frequencies so that an optimal use is made of the (limited) dynamic range of the A-to-D converter. It should be noted that the recorder exhibits appreciable losses at high frequencies. The quotient of largest

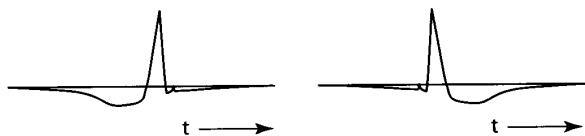


Fig. 1. Impulse response for normal play (left curve) and reverse play (right curve).

and smallest value of the signal's amplitude at the low and high end of the frequency range is about 35 dB. The pre-equalization makes it possible to use a 6-bit A-to-D converter without sacrificing too much quantization noise. The A-to-D converter's sampling frequency was chosen 3.2 times higher than the channel bit frequency. This relatively high over-sampling factor has been chosen to make it easier to recover the channel clock under adverse conditions. The signal processing steps, equalization, clock recovery, and data detection, following the A-to-D converter are entirely done in the digital domain. Once the signal is in the digital domain, the signal is filtered by a cascade of an IIR and FIR filter. The filters serve to compensate for the analog pre-equalization and also shape the overall response to the desired one. The desired response has a cosine^β shape given by the equation

$$H(\omega) = \cos^{\beta} \omega T_c,$$

where T_c denotes the channel bit interval. The value of $\beta = 3$ was chosen as it provides a good trade off between the jitter of zero crossings and the vertical eye opening. For a detailed description of channels with cosine^β response, the reader is referred to [7], volume II, Chapter 4. In [8], results, both experimental and theoretical, are provided of an advanced detection method, where the special attributes of the ETM code are exploited in order to improve the detection quality.

The equalization circuitry must cater for various different channel impulses. The tape passes the head in the same direction during recording and playback with consumer equipment as only one side is recorded at a time. During mass production of pre-recorded tape, both sides are recorded simultaneously at 64-fold speed. The asymmetry in the write process results in different channel impulse responses. The impulse response depends on the fact whether or not the tape has been pre-recorded. It also depends on the fact whether the head is fixed or rotated to read in the reverse direction. Typical impulse responses are displayed in Figure 1.

For specific portable applications, speed variations resulting from external shocks may cause severe difficulties for the clock recovery and other parts of the time-base correction. In the next section we will discuss in more detail how by a dedicated PLL design, these challenges

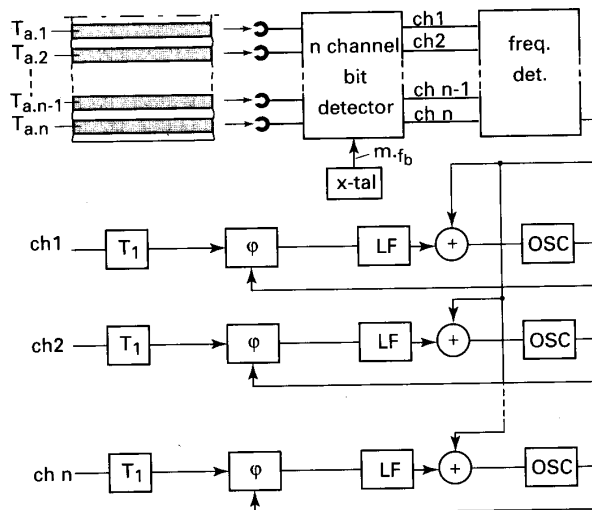


Fig. 2. Block diagram of the multi-track phase-lock loop. The circuitry consists of eight standard PLLs each with an extra input for the digitally controlled oscillators. An essential component of the multi-track PLL is the frequency detector. The time interval between zero crossings of the various equalized signals is used as a measure of the tape speed. The frequency detector combines the signals from all tracks. The output of the frequency detector is applied to the extra input. It can be seen that the frequency detector is not a part of the loop, and does, therefore, not affect the stability of the loop.

could be met.

IV. MULTI-TRACK PLL DESIGN

The relatively high over-sampling factor, 3.2, makes it very easy to accurately recover the data clock. (a clear disadvantage of the high over-sampling factor is that the power consumption of the relevant part of the electronics is proportionally higher.) Mechanical properties of the tape transport and tape elasticity may result in time-base errors between the individual tracks. The dynamic time-base difference of the two tracks furthest apart may easily amount to ten, or more, channel bit intervals. This makes it necessary to treat the tracks as eight independent recording channels. The deck electronics must therefore cater for eight different equalization circuits, PLLs etc. This is expensive and methods have been sought to overcome this. If it is assumed that the speed variations are the same for all the tracks, we can combine the values of the eight frequency detectors. Averaging over the eight values thus obtained yields a control signal which is a measure for the tape speed variation. A data clocking and detection system using the above feature is described

in [9]. Each track has a separate phase detector, and the phase errors are used to control a single common voltage controlled oscillator (VCO). The VCO provides clock pulses for all tracks thereby effecting a cost reduction. The VCO output is applied to the various phase detectors thereby creating a plurality of feedback loops. Each PLL should have a bandwidth narrow enough to be immune to the noise present, and, conversely, the bandwidth should be so large that it is capable of following the tape speed variations. In practice, a compromise bandwidth for the loop is determined for which the loop operates correctly under nominal conditions. However, we found that during periods of vibration or shocks, the loop discussed above frequently comes out of lock. In order to extend the response time of the PLLs, we decided to apply feedforward instead of feedback. It has been common practice to extend the lock-in range of the PLL by applying a signal proportional with the frequency difference of the input signal and the controlled oscillator. As in [9], we form a combined control signal. This control signal, which may be regarded as a frequency control signal, is, after low-pass filtering, applied to the voltage-controlled oscillators of all the PLLs. Since the information from all the eight tracks is used for this, it is possible to derive a control signal such that the loop responds more rapidly to speed variations. Unlike the PLLs [9], the control signal is applied to the PLLs in a feed-forward mode which has the great advantage that the arrangement cannot give rise to false-lock problems or deterioration of the signal-noise ratio owing to large bandwidths. A feed-forward control has the extra benefit that the response time can be much smaller than the response time of a feedback loop. As a result, the new PLL shows improved robustness against external disturbances such as shocks without sacrificing too much on its stationary behavior. Figure 2 shows the arrangement intended for reading a digital signal from a plurality of tracks. After amplification the signals are digitized. From each of the eight digital signals a clock frequency is derived for the purpose of bit detection. To this end, the signals are, after an appropriate delay, T_1 , applied to eight separate PLLs. The reason for inserting the delay will be discussed later. The output of the phase comparator φ is coupled to the input of a digitally controlled oscillator (OSC) via the loop filter (LF). The PLLs have an extra control input used for applying the control signal. The signal combination units may be constructed as digital adders. The new construction has the advantage that the bandwidth of the PLL can be comparatively small because speed variations are compensated by the additional control signal, which may be regarded as a frequency control system. The phase control loop merely has to compensate for the phase difference between the individual channels. This improves the stability behavior of the loops. Moreover, since eight times as many signal transitions are used to determine the additional control signal, the signal-noise ratio in this

control signal is higher. In order to remove residual noise, the control signal is low-pass filtered, which entails an inevitable delay of the control signal. The delay is inversely proportional to the bandwidth of the low-pass filter. The filter delay implies that the control signal is in fact always late with respect to shocks. This reduces the effect of the control signal. The filter delay is compensated by also delaying, see Figure 2, the phase signals prior to applying them to the PLL. In this way, the control signal arrives just in time to hit the time-base error on its nose.

V. CONCLUSIONS

We have presented the design considerations of the signal processing path of a multi-track stationary-head recorder. Ample experimental data have shown that time-base instabilities impose great challenges to the system architecture. Time-base instabilities may result in bit insertions or deletions, but they may also cause, for example during severe accelerations, data speed variations that may lead to complete loss of synchronization. We have presented a novel PLL design incorporating signals from a plurality of parallel tracks. The new multi-track PLL has shown an improved robustness against accelerations relative to traditional single-track designs.

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