

Novel Constrained Parity-Check Code and Post-Processor for Advanced Blue Laser Disk

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Abstract: Novel constrained parity-check code and post-processor are proposed for advanced blue laser disk systems. Simulation results with the blu-ray disc show that an increase of 5GB in capacity can be achieved over the standard system.

1. Introduction

Coding and signal processing have become increasingly important and powerful parts of optical recording systems. The reception techniques for blue laser disk systems (*i.e.* the blu-ray disc (BD) and high-definition digital versatile disc (HD-DVD)) are significantly different from that used in compact disc (CD) and DVD. For example, the threshold detector is replaced by more powerful Viterbi-like bit detectors, and the minimum runlength constraint is reduced from $d=2$ to $d=1$. Improvements have also been made in pre-processing, which increase the recording capacity of BD from the standard 23.3-25-27 GB to 35GB on a single layer [1].

In this paper, we propose an advanced detector with a novel capacity approaching constrained parity-check (PC) code and a multiple-error-event correction post-processor, for blue laser disk systems with even higher capacity. Fig. 1 shows the block diagram of a $d=1$ channel with PC code and post-processor. The $d=1$ constrained PC encoder adds a $d=1$ constraint and parity-check constraint on fixed-length segments of user data. Violation of the parity-check constraint in the detected bit sequence enables error detection. The task of locating the exact positions of the errors is done by a post-processor. In this way, dominant short error events at the output of the channel detector can be corrected by the PC code with very low redundancy, and the correction capacity loss of the outer error correction code (ECC) is reduced. Therefore, this approach provides an efficient solution to improve the overall performance, with affordable implementation complexity.

2. Novel capacity approaching constrained parity-check (PC) codes

Fig. 2 is a block diagram for encoding a constrained PC code in non-return-to-zero-inverse (NRZI) format. A M -bit segment of user data is first partitioned into $K+1$ data words. The K leading data words are encoded by the coding method proposed in [2], since the rates of the constructed codes are only a few tenths below the capacity. The obtained codewords are referred to as “normal constrained (NC) codewords”. The $(K+1)$ 'th data word is encoded by a novel parity-related constrained encoder, and the resulting codeword is referred to as the “parity-related constrained (PRC) codeword”. It is designed to realize a certain parity-check constraint over the combined codeword, which is a concatenation of the sequence of NC codewords and the PRC codeword. The parity-check constraint corresponds to a predetermined generator matrix (or generator polynomial), which is defined to detect any dominant error events or error event combinations in optical recording systems. For ease in imposing the modulation constraints, the generator matrix needs to be chosen or designed to generate a systematic PC code. This code design principle is based on the following proposition.

Proposition 1: Consider a $[j, i]$ systematic linear binary parity-check code C . Let \mathbf{u}_1 and \mathbf{u}_2 , respectively, denote row vectors with i_1 bits and $i_2 = i - i_1$ bits consisting of a sequence of NC codewords and a PRC codeword. If the parity bits of $[\mathbf{u}_1 \mid \underbrace{0, \dots, 0}_{1 \times i_2}]$ and $[\underbrace{0, \dots, 0}_{1 \times i_1} \mid \mathbf{u}_2]$ are equal, then the combined codeword $[\mathbf{u}_1 \mid \mathbf{u}_2]$, appended with $j - i$ bits of zeros, generates a codeword of C .

Proof: Let $\mathbf{G} = [\mathbf{I} \ \mathbf{P}]$ be a generator matrix that describes the encoder of C , where \mathbf{I} is an $i \times i$ identity matrix, and \mathbf{P} is an $i \times (j - i)$ matrix. The parity bits of $[\mathbf{u}_1 \mid \underbrace{0, \dots, 0}_{1 \times i_2}]$ and $[\underbrace{0, \dots, 0}_{1 \times i_1} \mid \mathbf{u}_2]$ are computed as $\mathbf{p}_1 = [\mathbf{u}_1 \mid \underbrace{0, \dots, 0}_{1 \times i_2}] \mathbf{P}$ and $\mathbf{p}_2 = [\underbrace{0, \dots, 0}_{1 \times i_1} \mid \mathbf{u}_2] \mathbf{P}$, respectively. If $\mathbf{p}_1 = \mathbf{p}_2$, we obtain $[\mathbf{u}_1 \mid \mathbf{u}_2] \mathbf{P} = [\underbrace{0, \dots, 0}_{1 \times (j-i)}]$. Thus, $[\mathbf{u}_1 \mid \mathbf{u}_2 \mid \underbrace{0, \dots, 0}_{1 \times (j-i)}]$ is a codeword

of C . □

During encoding, the K leading NC codewords are first constructed and connected. The parity bits of the sequence of NC codewords (appended with i_2 trailing bits of zeros) are then computed by a parity-check unit. The obtained parity bits are then passed to the PRC encoder, and a PRC codeword, which produces the same parity bits when appended with i_1 leading bits of zeros, is selected from a candidate codeword set. The PRC codeword is concatenated directly with the NC codewords and a N -bit constrained PC codeword is thus constructed. At the detector output, by checking the parity bits of the received constrained PC codeword, which are equal to the syndrome of the codeword (appended with $j - i$ bits of zeros), we can detect errors in the received codeword that are within the error detection capability of the corresponding PC code C .

The rate of the constrained PC code is given by

$$R = \frac{M}{N} = R_n - \frac{n}{N}(R_n - R_p), \quad (1)$$

where M , N and n are the length of the segment of user data, the combined constrained PC codeword, and the PRC codeword, respectively, and R_n and R_p are the rates of the NC code and the PRC code, respectively. The choice of N depends on the specific recording system and is a compromise between the code rate loss due to parity-check and the error correction capability of the post-processor.

In the design of the PRC code, we propose a novel approach to design sets of codewords with distinct parity bits, based on the same finite state machine (FSM) for designing the NC code [2]. This enables the two component codes to be connected in any order without violating the modulation constraints. Furthermore, since the PRC code part is also protected by parity-checks, error propagation is avoided. During decoding, the operation of the PRC decoder is generally the same as that of the NC decoder [2], but with the associated code tables being different. Using the above code design principle, efficient constrained PC codes can be designed either in NRZI format or in non-return-to-zero (NRZ) format. Designing the codes in NRZ format may reduce the number of parity bits required for error detection and simplify post-processing.

3. Multiple-error-event correction post-processor

The purpose of post-processor is to locate the exact locations of errors, by using the Viterbi output bits, the corresponding detector input samples and the parity-check result (*i.e.* syndrome of the detected codeword). The simple maximum-likelihood (ML) based matched-filtering type post-processor is widely used for the parity-check based post-processing, assuming that only one dominant error event is present in a detected codeword [3,4]. Obviously, the above single-error-event correction scheme may make mis-corrections when multiple error events occur within one codeword. In this paper, we propose a multiple-error-event correction post-processing scheme, which is summarized as follows. (i) For each of the matched-filter, the output samples are sorted in descending order of magnitude as candidate outputs. Several largest samples that satisfy the $d=1$ constraint are selected to indicate the candidate error events. We restore the corresponding error types, error locations, and syndromes. (ii) From the candidate error events obtained from Step (i), select single error events as well as various combinations of multiple error events that produce the same syndrome as the parity-check result. Furthermore, each pair of error events is separated by an interval that is larger than the error-free interval, which is the effective length of the channel memory. Several sets of candidate error events can be obtained. *e.g.* Candidate Event Set I contains the single error events, Candidate Event Set II contains various combinations of double error events, *etc.* (iii) Compute the squared Euclidean distance between the detector input samples and their re-constructed versions based on each error event or error event combination in the candidate event sets. The error event(s) with the minimum distance is determined as the most likely event(s). Since the number of candidate error events obtained from Step (ii) is quite limited after the first round screening done by the matched-filters, the complexity for correcting multiple error events is minimized.

4. Simulation results and discussion

The performance of the above new codes and post-processor is evaluated using BD systems. Similar performance can also be expected from HD-DVD systems. In the simulations, it is assumed that the optical read-out is linear and the Braat-Hopkins model [4,5] is used to describe the channel. In the model, the normalized cut-off frequency $\Omega_u = f_c T_u$, where f_c is the optical cut-off frequency and T_u is the duration of one user bit, is a measure of the recording density. For a system using a laser diode with wavelength λ and a lens with numerical aperture NA , we get $\Omega_u = 2 NA L_u / \lambda$, where L_u is the spatial length of one user bit. For BD systems with $\lambda = 405 \text{ nm}$, $NA = 0.85$, rate 2/3 17PP code, and at the nominal capacity of 25GB, we get $L_u = 111.75 \text{ nm}$, and $\Omega_u \approx 0.47$. Similarly, at the capacity of 30GB, we have $L_u = 93 \text{ nm}$ and $\Omega_u \approx 0.39$. In the performance evaluations, a Viterbi detector that is matched to a 7-tap optimized channel PR target is used as the channel detector [4]. The additive channel noise before equalization is assumed to be Gaussian and white. The dominant error events at the Viterbi detector output turn out to be $\pm\{2\}$, $\pm\{2,0,-2\}$ $\pm\{2,0,-2,0,2\}$, and $\pm\{2,0,-2,0,2,0,-2\}$.

Using the proposed code design method, a new (1,18) 4-bit constrained PC code defined by the generator polynomial of $g(x) = 1 + x + x^4$ is designed in NRZ format, which can detect all the above dominant error events of the system. The rate 9/13 (1,18), 5-state code proposed in [2] is used as the NC code, and a new rate 7/16 (1,18) 5-state PRC code is further designed, which achieves 1.375 channel bits per parity check. The codeword length N is chosen to be $N = 406$, and according to equation (1), the overall code rate is $R = 0.6823$. Note that the capacity of PC codes with $d=1$ constraint is given by $R_c = R_{c(1,\infty)} - p/N$, where $R_{c(1,\infty)} = 0.6942$, is the capacity of ($d=1, k=\infty$) codes, and p is the number of parity bits. Hence, the rate of the new code is only 0.3% below the capacity. For post-processing, a double-error-event correction post-processor is found to be sufficient for this study.

Fig. 3 illustrates the bit error rate (BER) comparison of the BD system with the standard 17PP code and with the new constrained PC code. Observe that at the capacity of 30 GB, compared with the performance of the system with 17PP code and without parity (Curve 1), the rate 9/13 code without parity (Curve 2) brings a performance gain of 0.8 dB at $\text{BER} = 10^{-5}$, due to its 3.85% higher code rate. The new constrained PC code with a double-error-event correction post-processor (Curve 4) outperforms that with a single-error-event correction post-processor (Curve 3), and achieves an overall performance gain of 1.7 dB. It is further observed that over a wide range of SNRs, the performance of the new code at capacity 30 GB (Curve 4) approaches that of 17PP code at capacity 25 GB (Curve 5). This shows that compared to the standard BD, an increase of 5 GB in capacity is achieved using the proposed new code and post-processor. Moreover, an approach of the kind proposed in this paper, when combined with advanced pre-processing schemes such as that in [1], has the potential to further increase the capacity of BD.

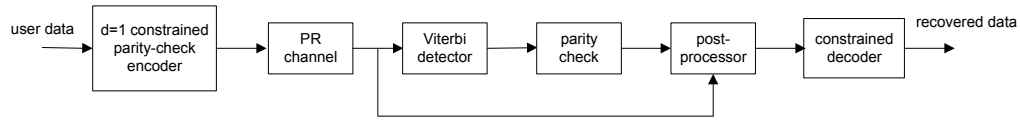


Fig. 1. Block diagram of $d=1$ channel with parity-check (PC) code and post-processor.

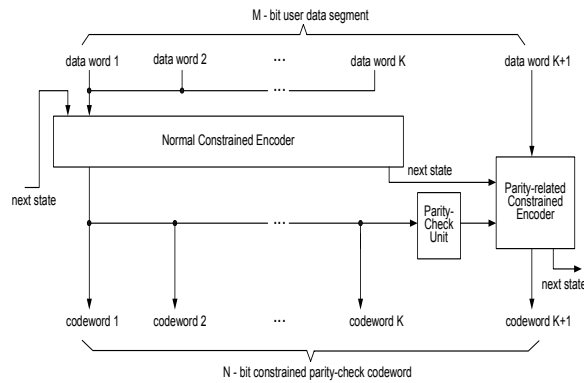


Fig. 2. Block diagram for encoding a constrained parity-check (PC) code in NRZI format.

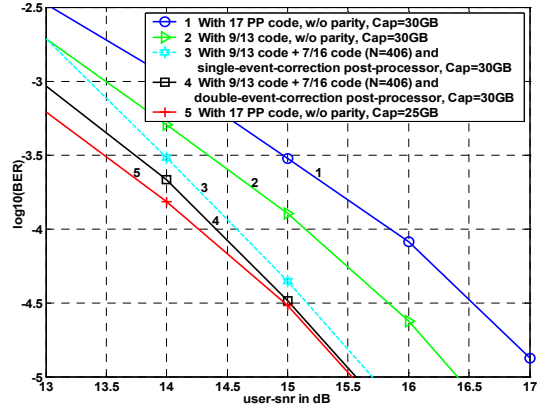


Fig. 3. BER comparison of BD system with the standard 17PP code and with the new constrained parity-check (PC) code.

5. Conclusions

In this paper, an advanced detection based on a novel capacity approaching constrained PC code and a multiple-error-event correction post-processor is proposed, which has the potential to increase the capacity by 5 GB over the standard BD. The implementation complexity of the proposed receiver is quite limited. Generalization of this scheme to HD-DVD is also straightforward.

References

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